LA-ispMACH 4000V/Z Automotive Family

3.3V/1.8V In-System Programmable SuperFAST™ High Density PLDs

July 2008 Data Sheet DS1017

Features

High Performance

- f_{MAX} = 168MHz maximum operating frequency
- t_{PD} = 7.5ns propagation delay
- Up to four global clock pins with programmable clock polarity control
- Up to 80 PTs per output

Ease of Design

- Enhanced macrocells with individual clock, reset, preset and clock enable controls
- Up to four global OE controls
- Individual local OE control per I/O pin
- Excellent First-Time-Fit™ and refit
- Fast path, SpeedLocking™ Path, and wide-PT path
- Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders

Zero Power (LA-ispMACH 4000Z)

- Typical static current 10µA (4032Z)
- 1.8V core low dynamic power
- LA-ispMACH 4000Z operational down to 1.6V

AEC-Q100 Tested and Qualified

- Automotive: -40 to 125°C ambient (T_A)

Easy System Integration

- Superior solution for power sensitive consumer applications
- Operation with 3.3V, 2.5V or 1.8V LVCMOS I/O
- Operation with 3.3V (4000V) or 1.8V (4000Z) supplies
- 5V tolerant I/O for LVCMOS 3.3, LVTTL, and PCI interfaces
- Hot-socketing
- Open-drain capability
- Input pull-up, pull-down or bus-keeper
- Programmable output slew rate
- 3.3V PCI compatible
- IEEE 1149.1 boundary scan testable
- 3.3V/2.5V/1.8V In-System Programmable (ISP™) using IEEE 1532 compliant interface
- I/O pins with fast setup path
- Lead-free (RoHS) package

Introduction

The high performance LA-ispMACH 4000V/Z automotive family from Lattice offers a SuperFAST CPLD solution that is tested and qualified to the AEC-Q100 standard. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the LA-ispMACH 4000V/Z architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The LA-ispMACH 4000V/Z automotive family combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

Table 1. LA-ispMACH 4000V Automotive Family Selection Guide

	LA-ispMACH 4032V	LA-ispMACH 4064V	LA-ispMACH 4128V
Macrocells	32	64	128
I/O + Dedicated Inputs	30+2/32+4	30+2/32+4/64+10	64+10/92+4/96+4
t_{PD} (ns)	7.5	7.5	7.5
t_S (ns)	4.5	4.5	4.5
t_{CO} (ns)	4.5	4.5	4.5
f_{MAX} (MHz)	168	168	168
Supply Voltage (V)	3.3V	3.3V	3.3V
Pins/Package	44-pin Lead-Free TQFP 48-pin Lead-Free TQFP	44-pin Lead-Free TQFP 48-pin Lead-Free TQFP 100-pin Lead-Free TQFP	100-pin Lead-Free TQFP 128-pin Lead-Free TQFP 144-pin Lead-Free TQFP

Table 2. LA-ispMACH 4000Z Automotive Family Selection Guide

	LA-ispMACH 4032Z	LA-ispMACH 4064Z	LA-ispMACH 4128Z
Macrocells	32	64	128
I/O + Dedicated Inputs	32+4	32+4/64+10	64+10
t_{PD} (ns)	7.5	7.5	7.5
t_S (ns)	4.5	4.5	4.5
t_{CO} (ns)	4.5	4.5	4.5
f_{MAX} (MHz)	168	168	168
Supply Voltage (V)	1.8V	1.8V	1.8V
Pins/Package	48-pin Lead-Free TQFP	48-pin Lead-Free TQFP 100-pin Lead-Free TQFP	100-pin Lead-Free TQFP

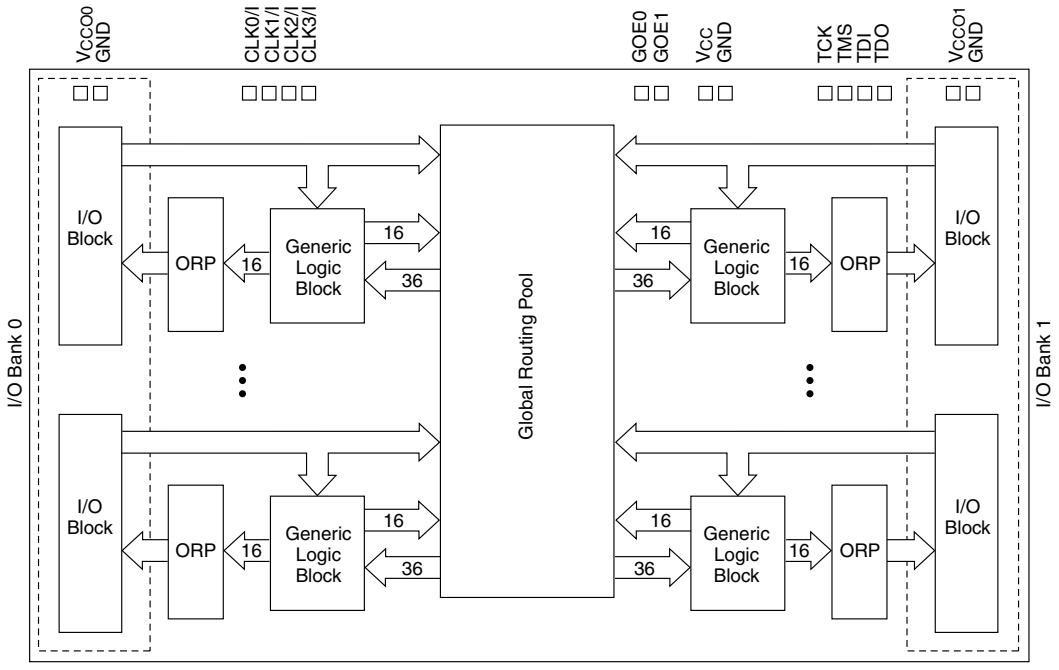
The LA-ispMACH 4000V/Z automotive family offers densities ranging from 32 to 128 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. Tables 1 and 2 show the macrocell, package and I/O options, along with other key parameters.

The LA-ispMACH 4000V/Z automotive family has enhanced system integration capabilities. It supports 3.3V (4000V and 1.8V (4000Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The LA-ispMACH 4000V/Z also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The LA-ispMACH 4000V/Z automotive family is in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to VCC (logic core).

Overview

The LA-ispMACH 4000V/Z automotive devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the LA-ispMACH 4000V/Z automotive devices are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

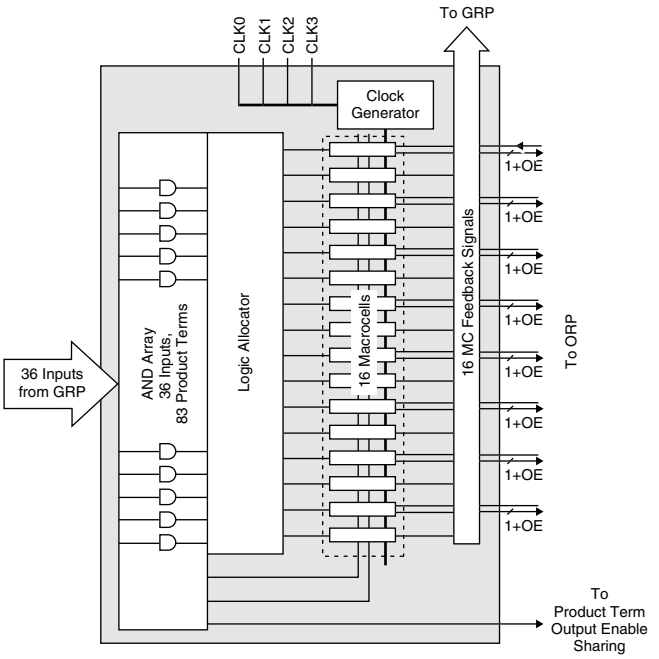
LA-ispMACH 4000V/Z Automotive Architecture

There are a total of two GLBs in the LA-ispMACH 4032V/Z, increasing to 8 GLBs in the LA-ispMACH 4128V/Z. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The LA-ispMACH 4000V/Z Automotive GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

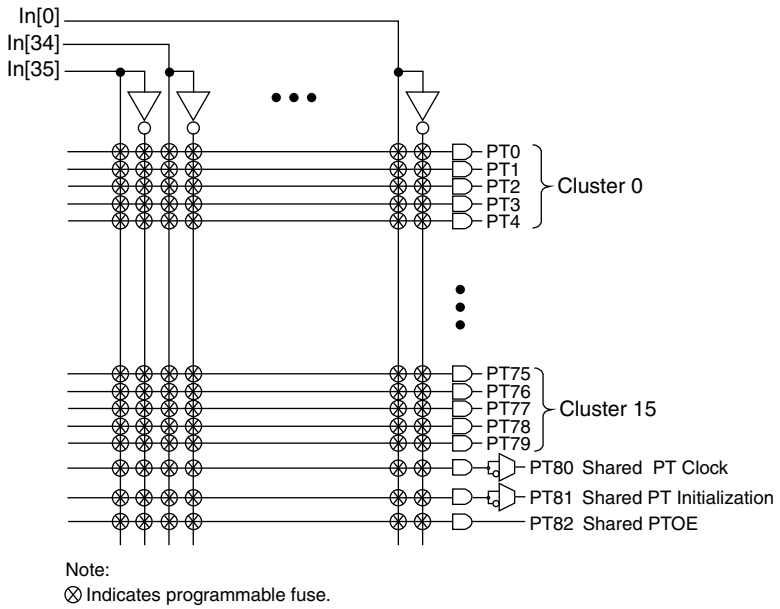


AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array



Note:
⊗ Indicates programmable fuse.

Enhanced Logic Allocator

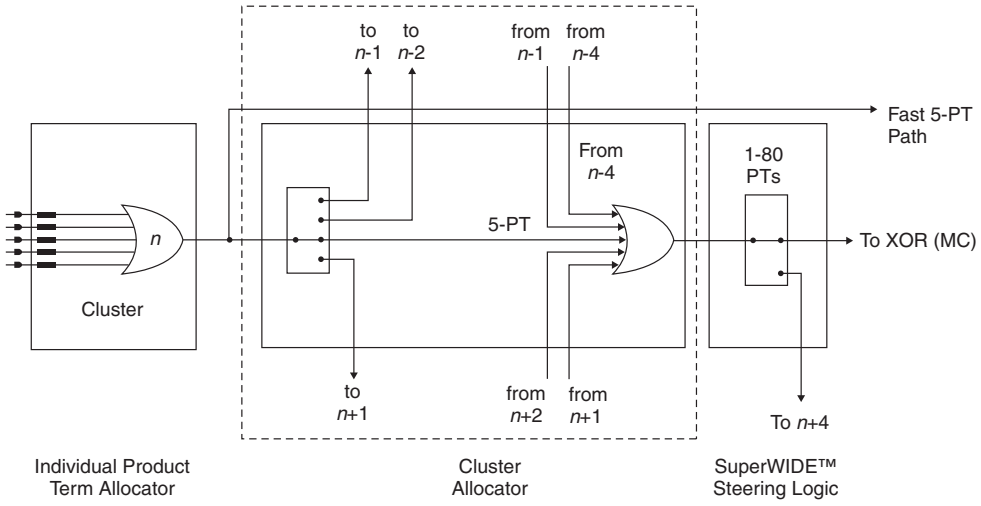
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the LA-ispMACH 4000V/Z automotive family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the LA-ispMACH 4000V/Z automotive family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 5 shows the product term chains.